Job Title	Senior DFT Engineer
Department	IC Design & Development
Reporting To	Manager – IC Design & Development
Location	Singapore
Position Summary	Performing IC DFT Development

Key Responsibilities

- Define SoC DFT architecture and DFM concept
- Implement and verify DFT measures to meet product specifications and production requirements
- Work closely with cross-function teams (design, production test and qualification) to meet test requirements with effective DFT solutions
- Achieve target coverage requirements for logic, memories, IO and mixed-signal IPs
- Generate test patterns and support post-silicon ATE and QnR
- Continue improving the DFT methods to optimize test time, IR-Drop and testability on internal and external IPs

Additional Responsibilities

- Any reasonable task assigned by management and deemed to be within the individuals' capabilities to ensure smooth running of the business.
- As this is an evolving business, ongoing change is an integral part of the position. Management will liaise with the individual on any fundamental change to work practices. The individual is required to embrace and adopt any change to working practices.

Knowledge & Skill Requirements

- Degree/Masters in Electrical/Electronic Engineering
- Minimum 5 years and above in the area of DFT and RTL design field.
- Expertise in ATPG scan, test controller, MBIST and their implementation
- Proficiency in HDL, synthesis, STA, top-level constraints and scripting
- Proficiency in EDA tools, e.g. VCS, TestMax DFT/ATPG/Advisor
- Strong analytical and problem-solving skills
- Experience on volume production will be added advantage
- Open and collaborative working style

Working Conditions

Working conditions are normal for an office environment with willingness to work in a flexible schedule. We provide a professional, fun and exciting work environment where innovation and creativity thrive!

Interested applicants email your CV along with a cover letter in Word or pdf format to **recruitment@brtchip.com**